

**METHOD FOR INTEGRATING NON-VOLATILE MEMORY WITH  
HIGH-VOLTAGE AND LOW-VOLTAGE LOGIC  
IN A SALICIDE PROCESS**

**ABSTRACT OF THE DISCLOSURE**

[0045] A method for integrating non-volatile memory with high-voltage and low-voltage logic in a salicide process is disclosed. The method includes forming a source region and a drain region associated with a gate region for each of a low-voltage (LV) device, a high-voltage (HV) device and a non-volatile memory (NVM) device. The HV, LV and NVM devices are electrically isolated by a field oxide region located adjacent to the respective source and drain regions. The field oxide regions are implanted with an isolation implant, such that the field implant is spaced a predetermined distance away from the HV and NVM source and drain regions. A blanking layer is deposited on the field oxide regions and a portion of the source and drain regions associated with the HV and NVM devices. Doped metal salicide regions are formed on the LV source and drain regions, all gate regions, and the exposed portions of the HV and NVM source and drain regions not covered by the blanking layer.